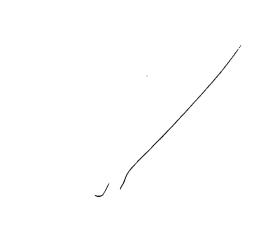
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A VHDL-based design methodology: the design experience of a high performance ASIC chip

Authors

Maurizio Valle Daniele Caviglia Marco Cornero Giovanni Nateri Luciano Briozzo 144

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SIGDA: ACM Special Interest Group on Design Automation

Publisher

IEEE Computer Society Press Los Alamitos, CA, USA

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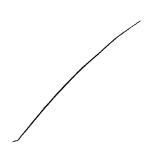
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Primary Classificati n:

B. Hardware

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European Design Automation Conference >archive Proceedings of the conference on European design automation conference >loc 1994, Grenoble, France

Scheduling of behavioral VHDL by retiming techniques

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N. Wehn

J. Biesenack

Peter Duzy

T. Langmaier

M. Münch

Michael Pilsl

S. Rumler

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SIGDA: ACM Special Interest Group on Design Automation

Publisher

IEEE Computer Society Press Los Alamitos, CA, USA

Pages: 546 - 551 Series-Proceeding-Article

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Annual ACM IEEE Design Automation Conference >archive Proceedings of the 28th conference on ACM/IEEE design automation conference >toc 1991, San Francisco, California, United States

Scheduling for functional pipelining and loop winding

Authors

Cheng-Tsung Hwang Yu-Chin Hsu Youn-Long Lin

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SIGDA: ACM Special Interest Group on Design Automation

IEEE-CS: Computer Society

Publisher

ACM Press New York, NY, USA

Pages: 764 - 769 Series-Proceeding-Article

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Citation

Annual ACM IEEE Design Automation Conference >archive Proceedings of the 29th ACM/IEEE conference on Design automation conference >toc

1992, Anaheim, California, United States

High-level synthesis from VHDL with exact timing constraints

Authors

A. Stoll

P. Duzy

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EDAC: Electronic Design Automation Consortium

IEEE-CS: Computer Society IEEE-CAS: Circuits & Systems

SIGDA: ACM Special Interest Group on Design Automation

Publisher

IEEE Computer Society Press Los Alamitos, CA, USA

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Annual ACM IEEE Design Automation Conference >archive Proceedings of the 28th conference on ACM/IEEE design automation conference >toc 1991, San Francisco, California, United States

CHOP: A constraint-driven system-level partitioner

Authors

Kayhan Kükçakar Alice C. Parker

Sponsors

SIGDA: ACM Special Interest Group on Design Automation

IEEE-CS: Computer Society

Publisher

ACM Press New York, NY, USA

Pages: 514 - 519 Series-Proceeding-Article

Year of Publication: 1991 ISBN:0-89791-395-7

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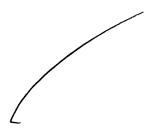


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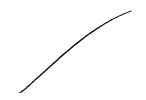
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2	System partitioning and timing analysis: A strongly polynomial-time algorithm for over-constraint resolution: efficient debugging of timing constraint violations Ali Dasdan Proceedings of the tenth international symposium on Hardware/software codesign May 2002 A system of binary linear constraints or difference constraints (SDC) contains a set of variables that are constrained by a set of unary or binary linear inequalities. In such diverse applications as scheduling, interface timing verification, real-time systems, multimedia systems, layout compaction, and constraint satisfaction, SDCs have successfully been used to model systems of both temporal and spatial constraints. Formally, SDCs are modeled by weighted, directed (constraint) graphs. The cons	77%

3 Instruction generation for hybrid reconfigurable systems

R. Kastner, A. Kaplan, S. Ogrenci Memik, E. Bozorgzadeh ACM Transactions on Design Automation of Electronic Systems (TODAES) October 2002

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TI: VHDL for High-Level Synthesis of Digital S /stems

Source: Proceedings of conference as follows fro n Dialog 165, Eventline: EVENT TITLE: 1st European Working Conference on VHDL Methods

EVENT DATE(S): September 4-7, 1990

Inst. Mediterraneen de Techn. HOST SITE:

EVENT CITY: Marseille **EVENT COUNTRY: France** ORGANIZER: Siemens

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